FIG. 1

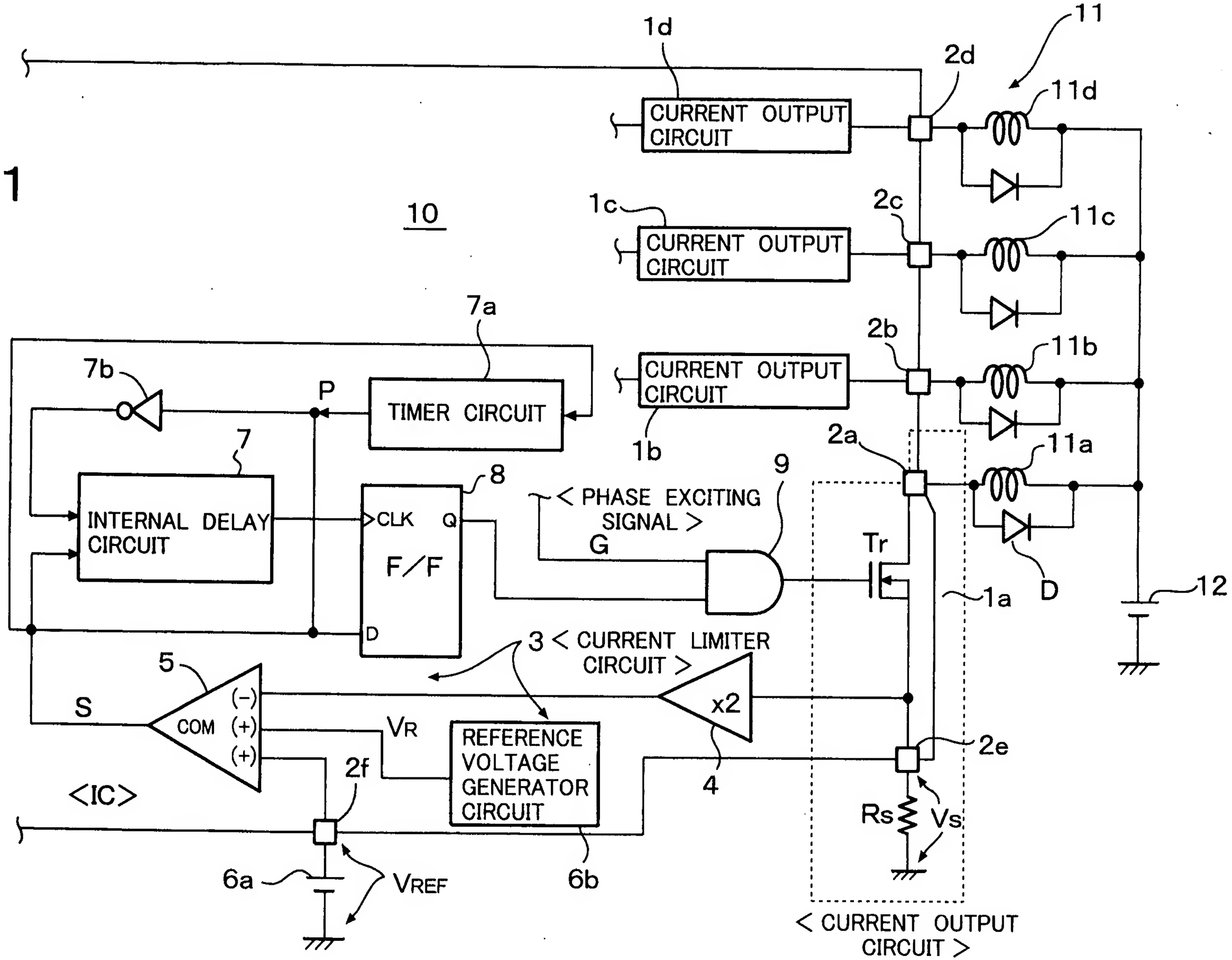
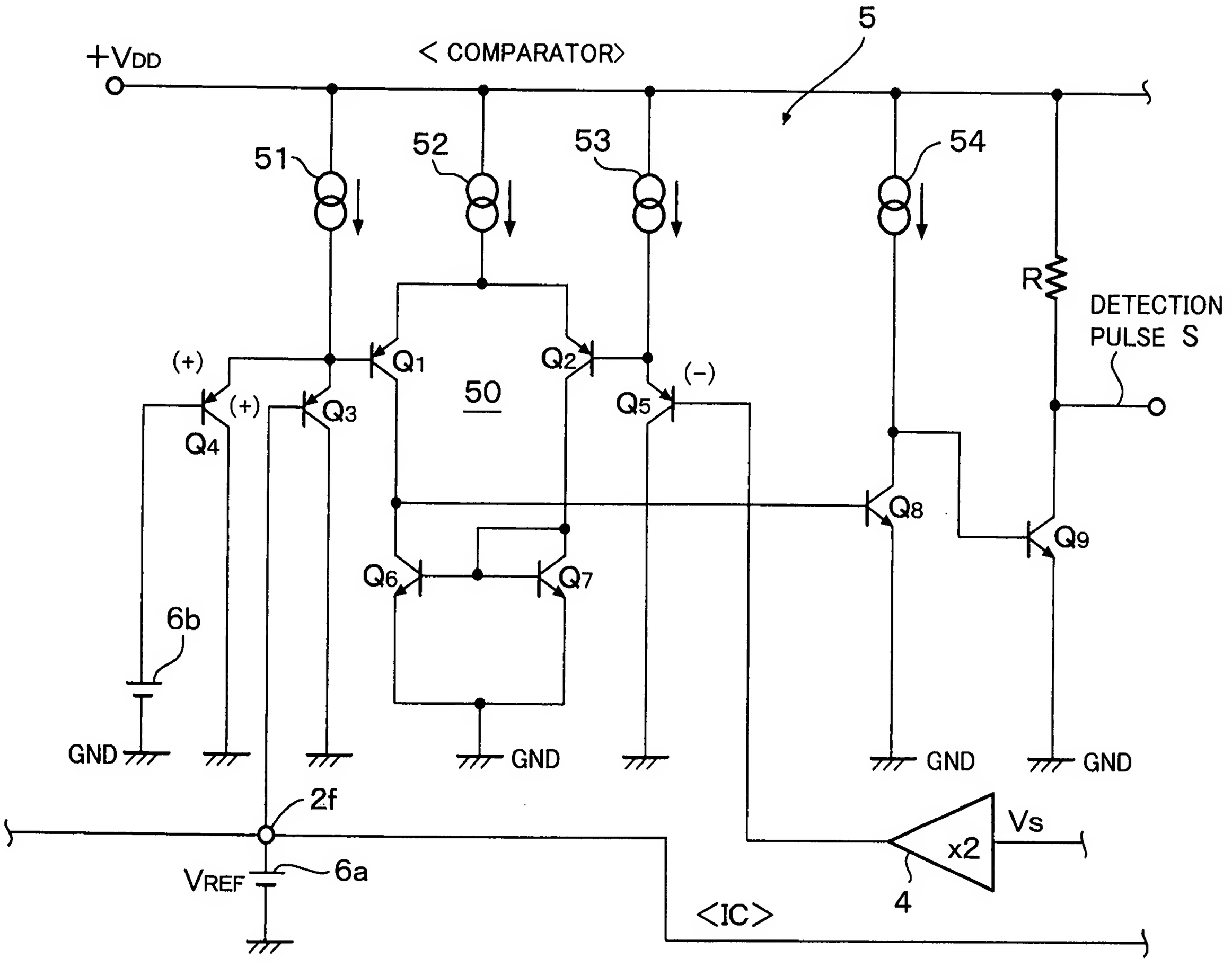

10
1d
2d
11
11d
CURRENT OUTPUT CIRCUIT
1c
2c
11c
CURRENT OUTPUT CIRCUIT
2b
11b
CURRENT OUTPUT CIRCUIT
1b
2a
11a
9
7a
7b
P
TIMER CIRCUIT
7
8
INTERNAL DELAY CIRCUIT
CLK
Q
F/F
D
< PHASE EXCITING SIGNAL >
G
Tr
D
1a
12
3 < CURRENT LIMITER CIRCUIT >
5
S
COM
(−)
(+)
(+)
x2
VR
REFERENCE VOLTAGE GENERATOR CIRCUIT
2e
4
2f
<IC>
Rs
Vs
6a
VREF
6b
< CURRENT OUTPUT CIRCUIT >

FIG. 2


+VDD
< COMPARATOR>
5
51
52
53
54
R
DETECTION
PULSE S
(+)
Q1
Q2
(-)
(+)
Q3
50
Q5
Q4
Q8
Q9
Q6
Q7
6b
GND
GND
GND
GND
2f
Vs
x2
VREF
6a
4
<IC>